

What is Claimed is:

1. An output driving circuit comprising:

a first level shifter for receiving an input signal to be provided to an outside of an integrated circuit and shifting a voltage level of the input signal to a voltage level required at the outside of the integrated circuit while maintaining a duty ratio of the input signal constant;

a second level shifter for receiving an output enable signal, and shifting a voltage level of the output enable signal to a voltage level required at the outside of the integrated circuit while maintaining a duty ratio of the output enable signal constant; and

an output driving unit for forwarding the input signal to the outside of the integrated circuit under the control of the output enable signal from the second level shifter.

2. The output driving circuit as claimed in claim 1, wherein the first or second level shifter includes;

an input signal splitting unit for providing the input signal in two signals having the same delay time periods,

a sense amplifier for amplifying voltage levels of the two signals into a voltage level required at the outside of the integrated circuit, and

a delay compensating unit for making delay time periods of the two signals amplified at the sense amplifier to be the same, and forwarding the two signals, selectively.

3. The output driving circuit as claimed in claim 2, wherein the input signal splitting unit includes;

first and second inverters for delaying the input signal for a preset time period and providing to one side input terminal of the sense amplifier, and

a first transmission gate for delaying a signal from the first inverter for a time period the same with a delay time period at the second inverter, and providing to the other side input terminal of the sense amplifier.

4. The output driving circuit as claimed in claim 2, wherein the sense amplifier includes a first PMOS transistor and a first NMOS transistor, and a second PMOS transistor and a second NMOS transistor, respectively connected in series between a power terminal the voltage level required at the outside of the integrated circuit is applied thereto and ground, for providing the voltage level of the power terminal and the voltage level of the ground, selectively.

5. The output driving circuit as claimed in claim 4, wherein the first NMOS transistor includes a gate connected to the second inverter, and serves as a first input terminal, and the second NMOS transistor includes a gate connected to the first transmission gate in the input signal splitting unit, and serves as a second input terminal.

6. The output driving circuit as claimed in claim 4, wherein the first PMOS transistor includes a gate connected to a connecting point of the second PMOS transistor and the second PMOS transistor, and the connecting point serving as the first output terminal of the sense amplifier, and

the second PMOS transistor includes a gate connected to a connecting point of the first PMOS transistor and a first NMOS transistor, the connecting point serving as the second output terminal.

7. The output driving circuit as claimed in claim 2, wherein the delay compensating unit includes a third PMOS transistor and a third NMOS transistor connected in series between the power terminal the voltage level required at the outside of the integrated circuit is applied thereto and ground, for providing the voltage level of the power terminal, and the voltage level of the ground, selectively.

8. The output driving circuit as claimed in claim 7, wherein the third PMOS transistor includes a gate connected to the first output terminal of the sense amplifier through a third inverter and a second transmission gate,

the third NMOS transistor includes a gate connected to the second output terminal of the sense amplifier through fourth and fifth inverters in succession, and

a connecting point of the third PMOS transistor and the third NMOS transistor connected to the output driving unit through the sixth inverter.

9. The output driving circuit as claimed in claim 2, wherein the first or second level shifter includes;

a seventh inverter for inverting the input signal,

a third transmission gate for delaying the input signal for a time period the same as the seventh inverter, and passing the delayed input signal,

third and fourth level shifters each for shifting a voltage level of a signal from the seventh inverter or the third transmission gate to a voltage level at the power terminal,

first and second pulse signal generating units each for generating a pulse signal at a rising edge of a signal from the third or fourth level shifter, and

an output signal generating unit for delaying signals from the first and second pulse

signal generating units for the same time periods, and generating signals having a high level voltage and a low level voltage shifted in response to the pulse signals generated at the first and second pulse signal generating units.

10. The output driving circuit as claimed in claim 9, wherein the third or the fourth level shifter includes;

a plurality of inverters for inverting and delaying the input signal in succession,

a sense amplifier for amplifying the inverted and delayed signal, and

a plurality of inverters for inverting and delaying the amplified signal in succession,

and providing to the output driving unit.

11. The output driving circuit as claimed in claim 10, wherein the sense amplifier includes a fourth PMOS transistor and a fourth NMOS transistor, and a fifth PMOS transistor and a fifth NMOS transistor respectively connected in series between the power terminal a voltage level required at the outside of the integrated circuit applied thereto and ground, for selectively providing the voltage level of the power terminal and the voltage level of the ground.

12. The output driving circuit as claimed in claim 11, wherein the PMOS transistor includes a gate connected to a connecting point of the fifth PMOS transistor and the fifth NMOS transistor,

the fifth PMOS transistor includes a gate connected to a connecting point of the fourth PMOS transistor and the fourth NMOS transistor, and

a connecting point of the fifth PMOS transistor and the fifth NMOS transistor serves

as an output terminal of the sense amplifier.

13. The output driving circuit as claimed in claim 9, wherein the first and the second pulse signal generating units generate pulse signals at falling edges of signals from the third and fourth level shifters, respectively.

14. The output driving circuit as claimed in claim 9, wherein the first or the second pulse signal generating unit includes;

a plurality of inverters for delaying and inverting a signal from the third or fourth level shifter, and

a NAND gate for subjecting the signal from the third or fourth level shifter, and a signal from the plurality of inverters to NAND operation.

15. The output driving circuit as claimed in claim 9, wherein the output signal generating unit includes;

an eighth inverter for inverting the input signal,

a fourth transmission gate for delaying the input signal for a time period the same with a delay time period at the eighth inverter, and passing the delayed input signal, and

a sixth PMOS transistor and a sixth NMOS transistor connected in series between the power terminal and the ground for providing the voltage level of the power terminal and the voltage level of the ground, selectively.

16. The output driving circuit as claimed in claim 15, wherein the output terminal of the third pulse signal generating unit is connected to a gate of the sixth PMOS transistor

through the eighth inverter,

the output terminal of the fourth pulse signal generating unit is connected to a gate of the sixth NMOS transistor, and

a connecting point of the sixth PMOS transistor and the sixth NMOS transistor is connected to a latch having a plurality of inverters.

17. The output driving circuit as claimed in claim 1, wherein the output driving unit includes;

an NAND gate for receiving for receiving signals from the first level shifter and the second level shifter, subjecting to NAND operation, and providing to a gate of the PMOS transistor,

an NOR gate for receiving signals from the first level shifter and the second level shifter, subjecting to NOR operation, and providing to a gate of the NMOS transistor,

a ninth inverter for receiving, inverting, and providing a signal from the second level shifter to the NAND gate, and

a seventh PMOS transistor and a seventh NMOS transistor connected in series between the power terminal and ground.